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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,987	03/16/2004	Yuko Fukawa	81872.0057	2506

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HOGAN & HARTSON L.L.P.
1999 AVENUE OF THE STARS
SUITE 1400
LOS ANGELES, CA 90067

EXAMINER	
TAI, XIUYU	
ART UNIT	PAPER NUMBER
1795	

NOTIFICATION DATE	DELIVERY MODE
05/28/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

laprosecution@hhlaw.com
ctkeyner@hhlaw.com
jalonso-sida@hhlaw.com

Office Action Summary	Application No.	Applicant(s)	
	10/801,987	FUKAWA ET AL.	
	Examiner	Art Unit	
	Xiuyu Tai	1795	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. The office action mailed on 12/8/2008 is withdrawn in light of the interview on 4/29/2009. This new office action is set forth to respond to applicant's argument filed on 3/4/2009.

2. Applicant's arguments, see REMARKS, filed 3/4/2009, with respect to claims 25-33 have been fully considered and are persuasive. The rejection of claims 25-33 under 35 U.S.C. 103(a) has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made.

Claim Rejections - 35 USC § 112

3. Claims 25-33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 25 recites the limitation "the second solder layer" in line 10. There is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.

5. Claim 25 recites the limitation of "an electrode" in line 9. It constitutes an indefinite subject matter. It is not clear what applicant regards as "an electrode" and the instant specification defines "a front surface electrode" and "a back surface electrode". Therefore, appropriate correction is required. For the purpose of examination, "an electrode" is interpreted as "the back surface electrode". Claims 26-33 are rejected because of their dependency and failure to remove the ambiguity of parent claim.

6. Claim 32 recites the limitation of "the electrode" in line 2. It is not clear which electrode it regards. Therefore, appropriate correction is required.

7. Claims 32 and 33 recite the limitation of "the solder layer". It is not clear if "the solder layer" refers to "the first solder layer" or "the second solder layer" since claim 25 recites two solder layers (i.e. a first solder layer and a second solder layer). Therefore, appropriate correction is required.

8. Claims 32 and 33 recite the limitation "a first solder layer" in line 4 and "a second solder layer" in line 5. It is not clear if they are the same as "a first solder layer" and "a second sold layer" as cited in claim 25. There is insufficient antecedent basis for this limitation in the claim.

9. Claim 32 recites the limitation "a first connection tab" in line 3. It appears that applicant has substituted "a first inner lead" with "a first connection tab" during prosecution. It is not clear if the applicant refers "a first connection tab" as another element that is different from "the first inner lead" or it is "the first inner lead". .Appropriate correction is required. For the purpose of examination, "a first connection tab" is interpreted as "the first inner lead".

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

13. Claims 25, 26, 32, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori et al (U.S. 5,718,772) in view of Asai et al (U.S.. 6,528,717) and in further view of Shiomi et al (U.S. 5,998,729).

14. Regarding claim 25, Mori et al disclose a method of making a solar cell module. Mori teaches to prepare solar cell module by (1) providing a photovoltaic element that has an upper electrode 204/205 on a semiconductor photovoltaic layer 203 and a lower electrode 201 (Figure 2; col. 10, line 61-66); and (2) connecting metal pieces such as

copper tabs 206 to the lower electrode 201 and the upper electrode 204 by soldering respectively (Figure 2; col. 12, line 12-19).

15. Mori does not teach to solder the upper electrode and the lower electrode with different solder layer nor a step of soldering the solder layer with a higher melting point first. However, Asai et al disclose a method of producing a photovoltaic panel. The method of Asai includes steps of (1) a first connecting step by soldiering the first solder layer 36 to the first electrode wherein the melting point of the first solder layer is about 245C (col. 10, line 1-10); and (2) a second connecting step by soldering the second solder layer 54 to the second electrode wherein the melting point of the second solder layer is about 157, after the first connecting step performed (col. 12, line 25-35). Asai indicates that soldiering higher melting point solder layer first is advantageous because it will prevent the connection on the first electrode from being molten again during the second connecting step (col. 11, line 5-10 & col. 12, line 35-40). Therefore, it would be obvious for one having ordinary skill in the art to solder the soldering layer with higher melting point before the lower melting point as suggested by Asai in order to ensure the connection between electrode and metal pieces while producing the solar cell module using the method of Mori. Moreover, Asai teaches two different solder layers: the first solder layer with higher melting point containing tin and silver (col.10, line 1-3) and the second solder layer with lower melting point containing lead, silver, and indium (col. 12, line 31-33).

16. Mori/Asai discloses the claimed invention except for a metal foil for connecting leads. Shiomi disclose a solar cell module that utilizes a copper foil as connecting lead

to the electrodes (col. 13, line 35-55). Shiomi shows that a copper foil is an equivalent connecting lead known in the art. Therefore, one having ordinary skill in the art would have found it obvious to substitute a copper foil for the copper tab.

17. Regarding claim 26, Asai teaches two different solder layers: the first solder layer with higher melting point containing tin and silver (col.10, line 1-3), reads on the instant claim.

18. Regarding claims 32 and 33, Asai teaches to form coating of solder layer on the conductive layer/electrode before soldering electrode with solder layer (col. 9, line 65-67), reads on the instant claim.

19. Claims 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori et al (U.S. 5,718,772) and Asai et al (U.S.. 6,528,717) and Shiomi et al (U.S. 5,998,729) as applied to claim 25 above, and in further view of Okada et al. (US Patent 6,571,469).

20. Regarding claim 27, Mori/Asai/Shiomi fails to teach that the connections are through holes/ the common connection line at the connection areas between the connection members and electrodes. However, Okada et al. disclose a soldering method (Figure 26) for the manufacture of a modular board (Figure 1) with multiple electrodes. The method includes the use of through-holes 103 in order to bond electrodes more securely even when the board is subject to wrapage (col.1, lines 63-65 & col. 2, lines 1-10). The through-holes allow molten solder to flow freely between the two electrodes to create a more reliable contact (col. 3, lines 45-48). Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention to use

the soldering method along with the through holes as suggested by Okada in order to bond the surface of the connection members to electrodes of Mori/Asai/Shiomi more reliably (i.e., more securely even when the electrodes are subject to wrapage) by allowing molten solder to flow more freely between them.

21. Regarding claim 28, Mori/Asai/Shiomi fails to teach that the connections are the common connection line at the connection areas between the connection members and electrodes. However, Okada et al. disclose a soldering method (Figure 26) for the manufacture of a modular board (Figure 1) with multiple electrodes. The method includes the use of through-holes 103 in order to bond electrodes more securely even when the board is subject to warpage (col.1, lines 63-65 & col. 2, lines 1-10). The through-holes allow molten solder to flow freely between the two electrodes to create a more reliable contact (col. 3, lines 45-48). Therefore, it would also have been obvious to one of ordinary skill in the art at the time of the invention to use the soldering method along with the through holes as suggested by Okada in order to bond the surface of the connection tab to the surface of the connection line of Mori/Asai/Shiomi more reliably (i.e., more securely even when the electrodes are subject to warpage) by allowing molten solder to flow more freely between the connection areas between the connection tabs and the connection line .

22. Regarding claim 29, Moir/Asai/Shiomi fails to teach that the common connection line is provided with through holes at connection areas between the common connection line and the connection tabs. However, Okada et al. disclose a soldering method (Figure 26) for the manufacture of a modular board (Figure 1) with multiple

electrodes. The method includes the use of through-holes (through holes, 103) in order to bond said electrodes more securely even when the board is subject to warpage (col.1, lines 63-65 & col. 2, lines 1-10). The through-holes allow molten solder to flow freely between the two electrodes to create a more reliable contact (col. 3, lines 45-48). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the soldering method along with the through holes as suggested by Okada in order to bond the surface of the connection tab to the surface of the connection line to each other more reliably (i.e., more securely even when the electrodes are subject to warpage) by allowing molten solder to flow more freely between them to the method of Mori/Asai /Shiomi for producing the solar cell module.

23. Claims 30, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori et al (U.S. 5,718,772) and Asai et al (U.S.. 6,528,717 and Shiomi et al (U.S. 5,998,729)) as applied to claim 25 above, and in further view of Mizukami et al. (US Patent 6,369,315) and Okada et al.(US Patent 6,571,469).

24. Regarding claims 30, and 31, Mori/Asai/Shiomi fails to teach a terminal box or output wires used to connect the solar cell elements to the terminals of that box. However, Mizukami et al. disclose a power generation system specifically for use with an array of photovoltaic modules (Figure 1). Mizukami et al. connect their photovoltaic array via bus bars 13 containing extensions 13b that are connected directly to an output fetching line (or a line that allows the power outputted by the cells to be used by the outside world) via a terminal box 17 (Figure 1; col. 5, lines 24-28) and the output wires (bus bar extensions, 13b) connect the solar cell elements with the terminals 18 of a

terminal box 17 by means of solder 23 (Figure 1; col. 5, lines 32-35). Mizukami further indicates that using a terminal box allows the number of soldering spots in an output fetching wiring to be reduced (col. 2, lines 5-10). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to add the bus bar extensions and the terminal box as suggested by Mizukami in order to reduce the number of soldering spots in output fetching wiring while using the method of Mori/Asai/Shiomi

Furthermore, Mori/Asai/Shiomi/Mizukami fails to teach that the output wires or the terminals of the box are provided with through holes at connection areas between the terminals and the output wires. However, Okada et al. disclose a soldering method (Figure 26) for the manufacture of a modular board (Figure 1) with multiple electrodes. The method includes the use of through-holes (through holes, 103) in order to bond said electrodes more securely even when the board is subject to warpage (col.1, lines 63-65 & col. 2, lines 1-10). The through-holes allow molten solder to flow freely between the two electrodes to create a more reliable contact (col. 3, lines 45-48). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the soldering method along with the through holes suggested by Okada while providing the through holes either the output wires or the terminals of Mori/Asai/Shiomi/Mizukami in order to bond the surface of the wire to the surface of the terminals to each other more reliably (i.e., more securely even when the electrodes are subject to warpage) by allowing molten solder to flow more freely between them.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Xiuyu Tai whose telephone number is 571-270-1855. The examiner can normally be reached on Monday - Friday, 7:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alexa Neckel can be reached on 571-272-1446. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/X. T./
Examiner, Art Unit 1795

5/11/2009

/Alexa D. Neckel/

Supervisory Patent Examiner, Art Unit 1795